

# The Machine: The future of technology

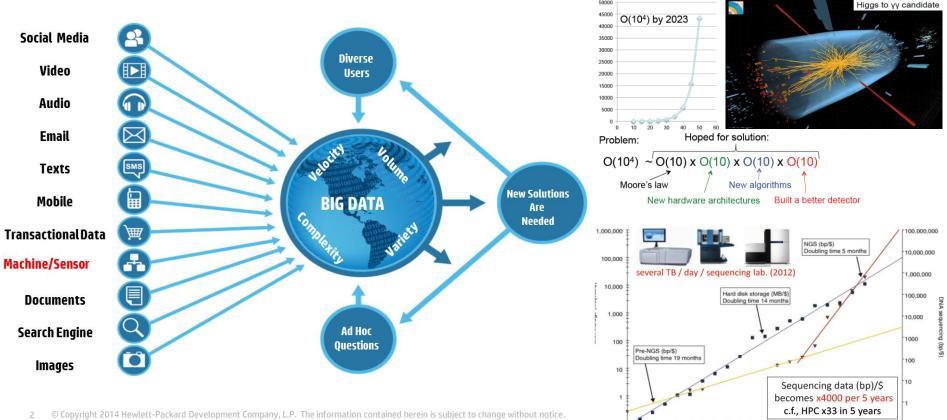
patrick.demichel@hp.com Hyperscale Division EMEA

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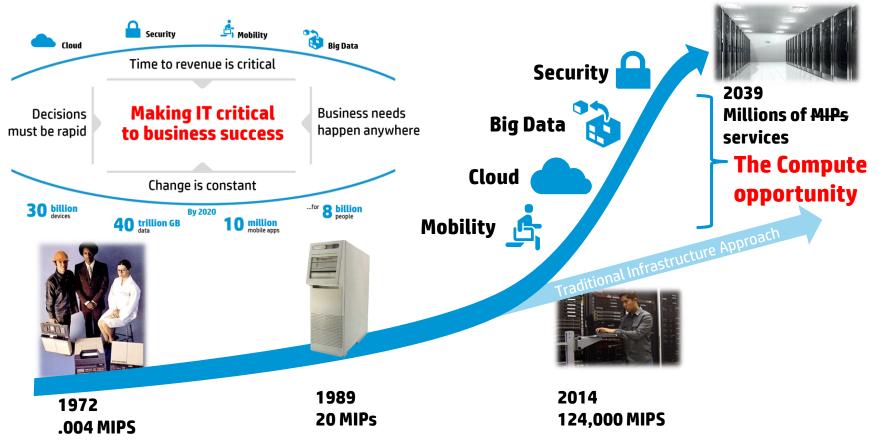
# Tsunami of data on the horizon

202X will be the decade of Extreme Data; massive compute is required for Extreme Analytics



Lincoln Stein, Genome Biology, vol. 11(5), 2010

## A new IT age is dawning: can you realize the benefits?



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## Today's computing infrastructure unable to keep up



You won't be able to get more capacity for less



Big Data will be too big to extract meaning from



You won't be able to move your data from where it's created – useful data may get ignored or discarded



By the time you've analyzed your data – it will be out of date

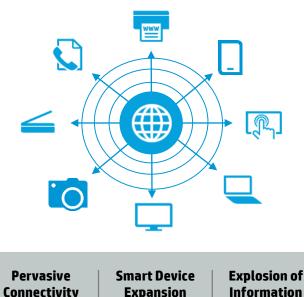


Your infrastructure will require more resources than you can get

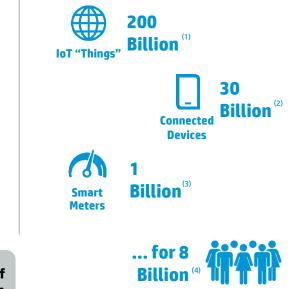


Securing your enterprise will take more computing resources than you have

### **Internet of Things**



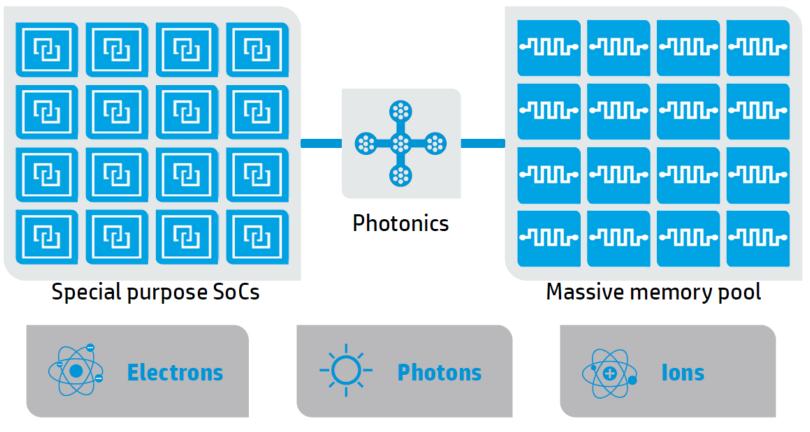
### **By 2020**



(1) IDC "Worldwide Internet of Things (IoT) 2013-2020 forecast" October 2013. (2) IDC "The Digital Universe of Opportunities: Rich Data and the Increasing Value of the Internet of Things" April 2014 (3) Global Smart Meter Forecasts, 2012-2020. Smart Grid Insights (Zypryme), November 2013 (4) http://en.wikipedia.org



# 3 disruptive technologies to the rescue



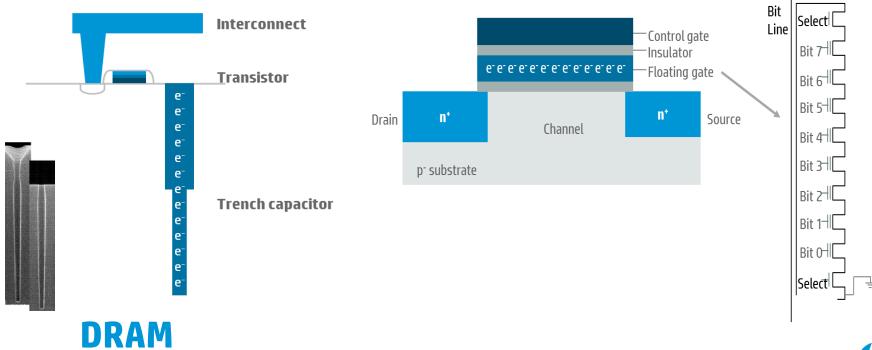
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# Memory scaling challenges





Flash





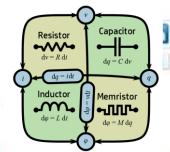
# Disruption #1: Non-volatile memories

### Breakthrough in storage and memory technology

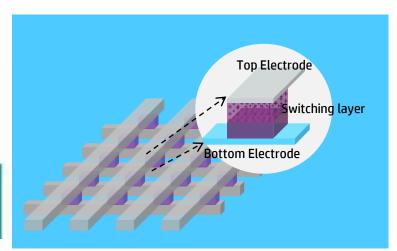
#### Scientists Create First Memristor: Missing Fourth Electronic Circuit Element

By Bryan Gardiner 🔄 April 30, 2008 ( 10:03 am ) Categories: Uncategorized Cline Send Statikes. Sign Up to see what your friends like.

Researchers at HP Labs have built the first working prototypes of an important new electronic component that may lead to instant-on PCs as well as analog computers that. process information the way the human brain does.





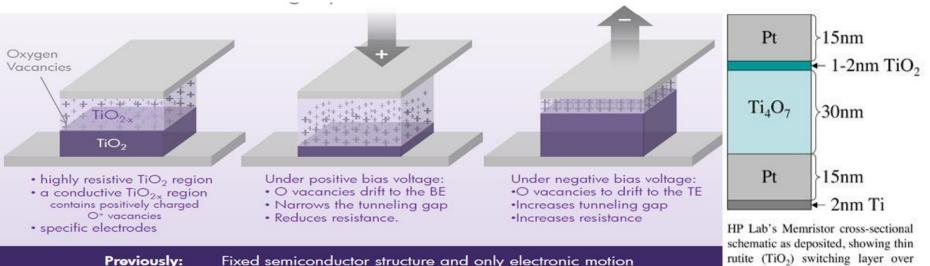


Technology	Density	Bandwidth	Latency	Latency	Energy	Energy	ς
	(µm²/bit)	(GB/s)	Read (ns)	Write (ns)	Read (pJ/b)	Write (pJ/b)	
Hard Disk	N/A	0.5	3,000,000	3,000,000	2500	2500	ח
Flash SSD [3] [6]	0.0021	1.0	25,000	200,000	250	250	
DRAM [6] [30]	0.0038	51.2	55	55	24	24	1
PCRAM (22nm) [30]	0.0058	variable	48	150	2	19.2	•
Memristor (22nm) [8]	0.0048	variable	100	100	1-3	1-3	

Store large amounts of data permanently like hard disks, but 00.000 times faster, and at much ower energy



## How does it work? Semiconducting bipolar switch



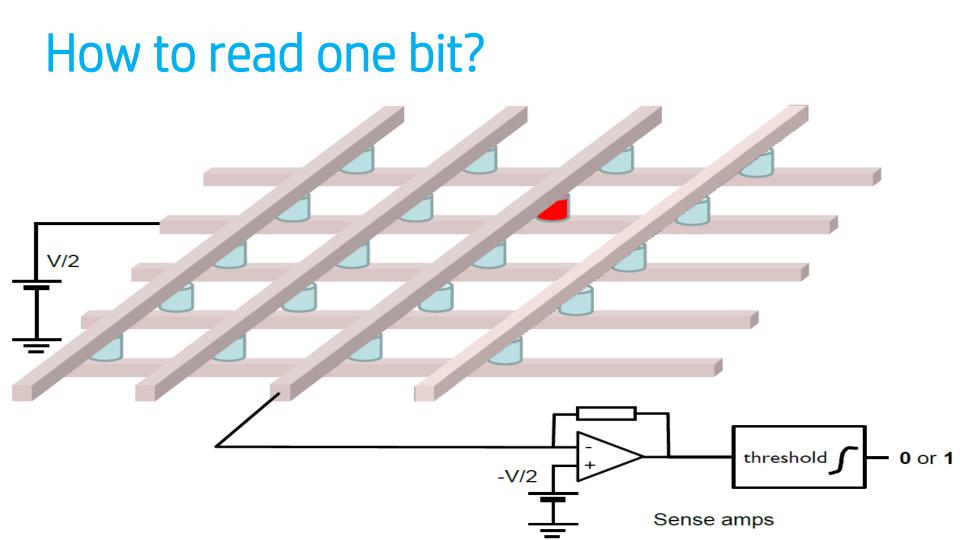
Now:

lonic motion dynamically modulates the semiconductor structure controlling the electronic current.

thicker magneli phase (Ti<sub>4</sub>O<sub>7</sub>) oxygen vacancy donor layer.

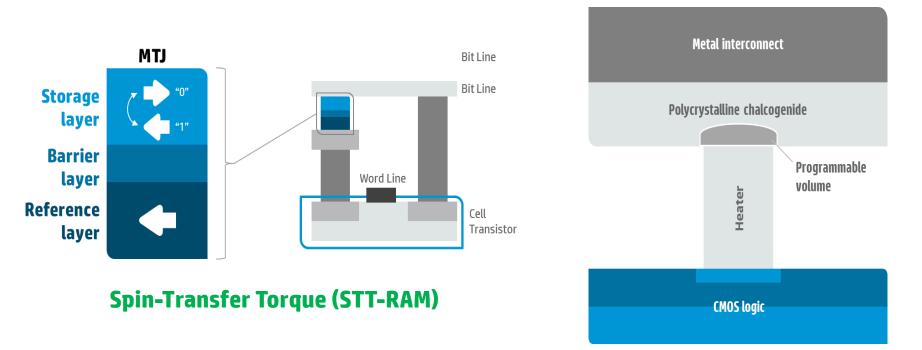
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# Other NVM Technologies

## Phase-Change (PCM)

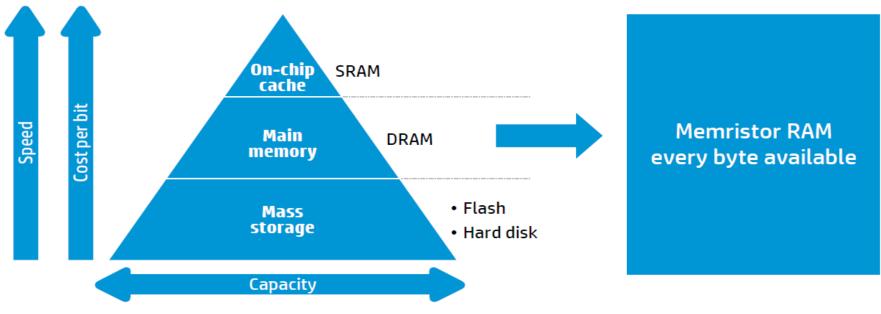




## UNIVERSAL MEMORY

Massive memory pool

A drastic reduction of the memory stack complexity and cost But requires a complete software stack redesign to leverage the full potentiality of the new architecture



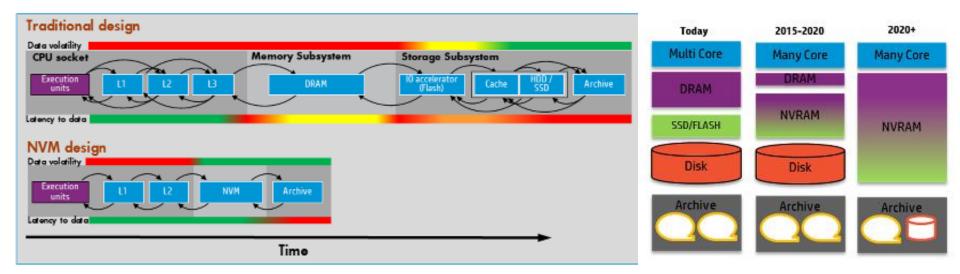
## Memristors change how and where data are stored



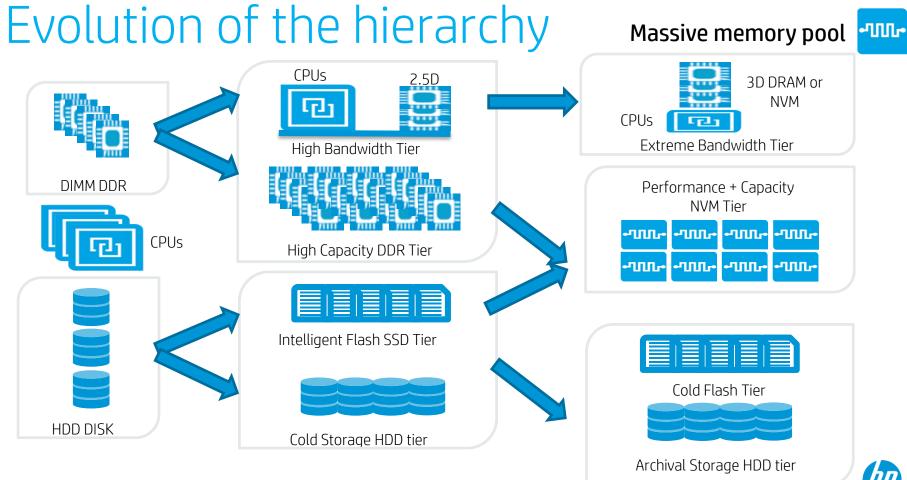
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# Memory Hierarchy As NVM Replaces DRAM

#### Step wise memory evolution to NVM



- Traditional API's designed to hide long device latencies and complex memory hierarchies will become obsolete. NVM Data Analytics can be done in-memory
- Applications such as relational databases that are structured to manage the long latencies to disk and the volatility of DRAM will be replaced by new technologies such as in-memory databases.





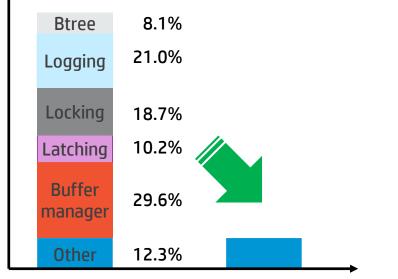
## Benefits of universal memory

Example: a database transaction

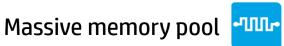
Traditional databases struggle with big & fast data

90% of a database transaction is overhead

### Memory-semantics nonvolatile memory: up to 10x improvement

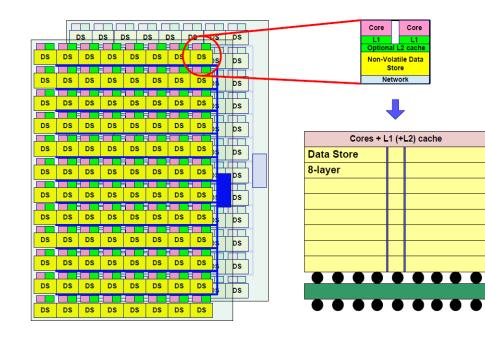


Source: S. Harizopoulos, D. Abadi, S. Madden, and M. Stonebraker, "OLTP Through the Looking Glass, and What We Found There," *Proc. SIGMOD*, 2008.





## Nanostores: in-memory compute



Flat converged storage hierarchy with compute colocation for 10x-100x improvement in performance per Watt

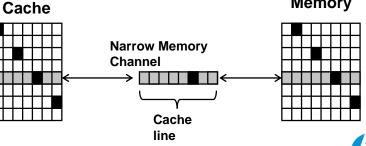
#### **Example: Matrix Computation**

for (i = 0; i < n; i++)

sum += A[i][i];

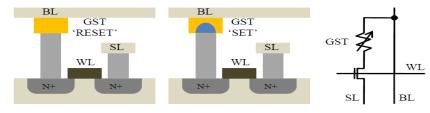
CPU

Physical Memory



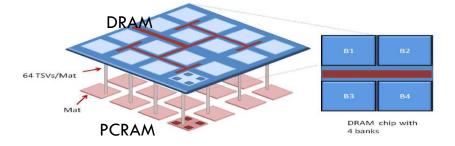
## Technologies for Check-point Restart www.nd.edu/~rich/SC09/tut157/SC2009\_Jouppi\_Xie\_Tutorial\_Final.pdf PCRAM



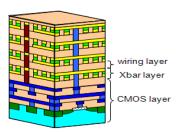


The schematic view of a PCRAM cell with NMOS access transistor (BL=Bitline, WL=Wordline, SL=Sourceline)

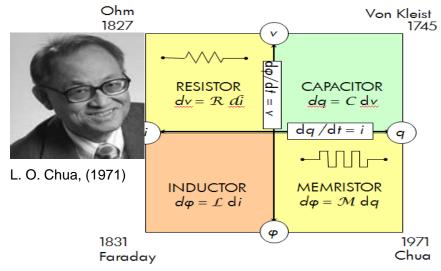
	HDD	NAND Flash	PCRAM
Taille cellule	-	4-6F^2	4-6F^2
Cycle lecture	~4ms	5us-50us	10ns-100ns
Cycle écriture	~4ms	2ms-3ms	100-1000ns
Watt à arrêt	~1W	~0W	~0W
Endurance cycles	10^15	10^5	10^8



CMOS chip avec des composants memrésistifs







# Why photonics?

FLOPs will cost less than on-chip data movement! (NUMA)









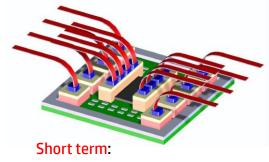
## Photonics technologies Communication fire hose for memristor stores

## **Why Photonics?**

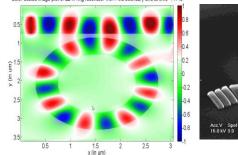
- Huge increases in the volume of data
- Enables efficient access to that data
- Shrink *time* and *space* to gain immediate access without regard for location

# Transmit data using light for 30-fold more bandwidth at one-tenth the energy





short range, low cost VCSEL

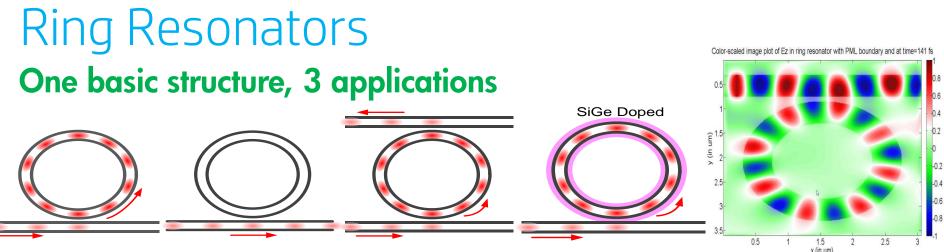




Long term: micro-ring resonator

(low cost, long distance, integrated on silicon)





A modulator – move in and out of resonance to modulate light on adjacent waveguide

A switch – transfers light between waveguides only when the resonator is tuned

A wavelength specific detector - add a doped junction to perform the receive function

## Microrings Full link configuration

### Advantages

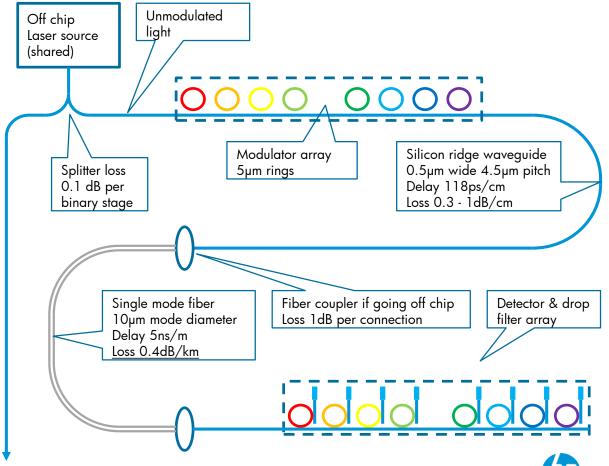
Modulators wavelength specific, no additional mux

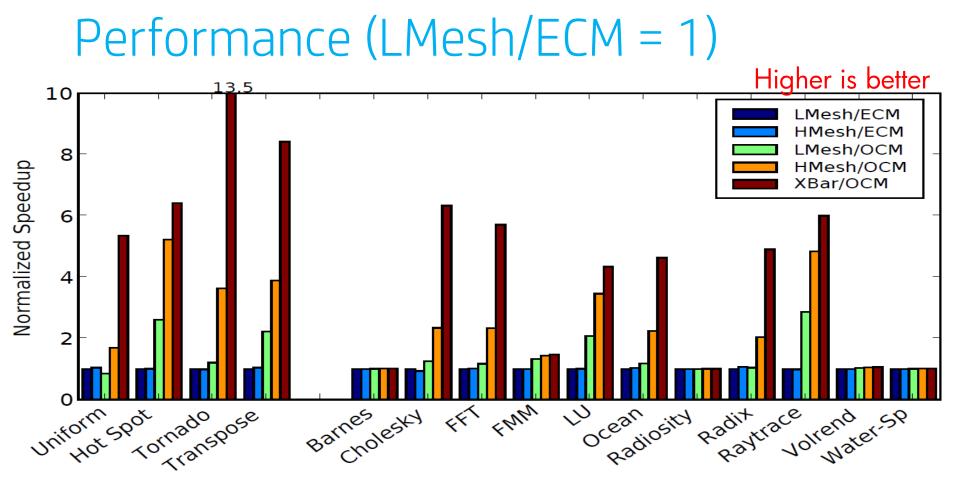
Same ring structure used for drop filters

Loss budget dominated by cost Up to 64 wavelengths

## **Outstanding issues**

Ring tuning Thermal stability

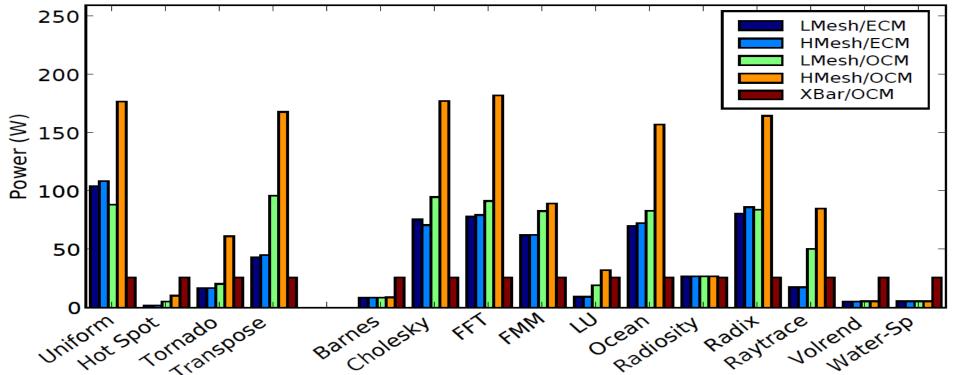




Applications that don't fit in cache show 4-6X improvements with Xbar

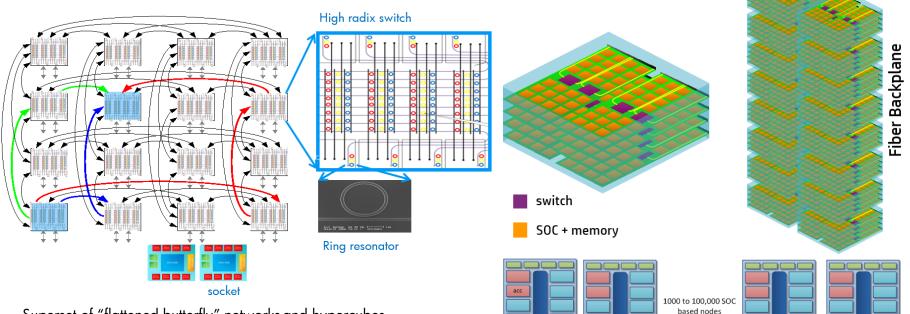
## **On-chip Network Power**

Lower is better



Optics can reduce network power of applications that don't fit in cache by 6X

## HyperX<sup>1</sup> fabric Fully connected sub-networks in multiple dimensions



- Superset of "flattened butterfly" networks and hypercubes
- Fully connected networks offer lowest hop count but limited scalability
- Multiple dimensions increase scalability at the expense of hop count
- Many alternate paths with one or more additional hop
- Non-minimal routes required for full bisection bandwidth

©2010 HP Confidential 1. "HyperX: Topology, Routing, and Packaging of Efficient Large-Scale Networks" Ahn et al., Supercomputing 2009

Fabric

high radix switches

switch network

high radix switches

high radix switches

high radix switches

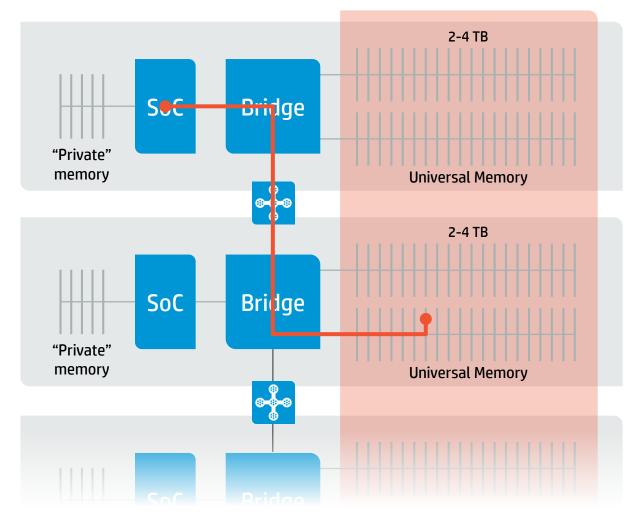




## **Photonics destroys distance**



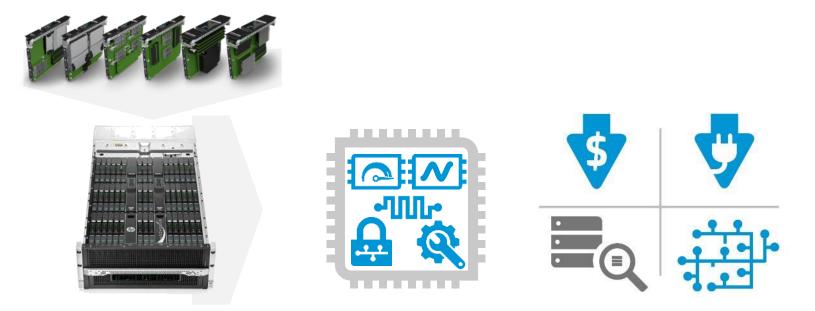
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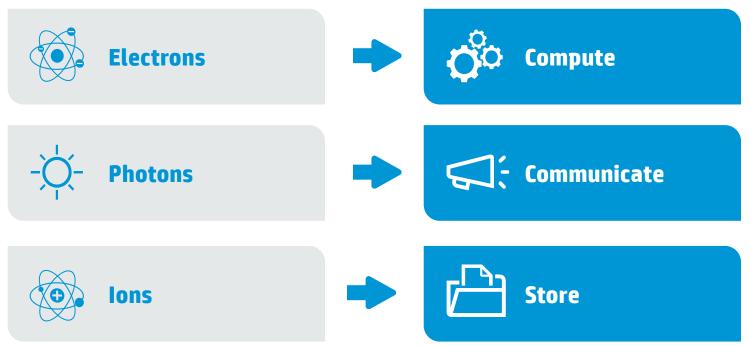




## **Customize the hardware to the workload**

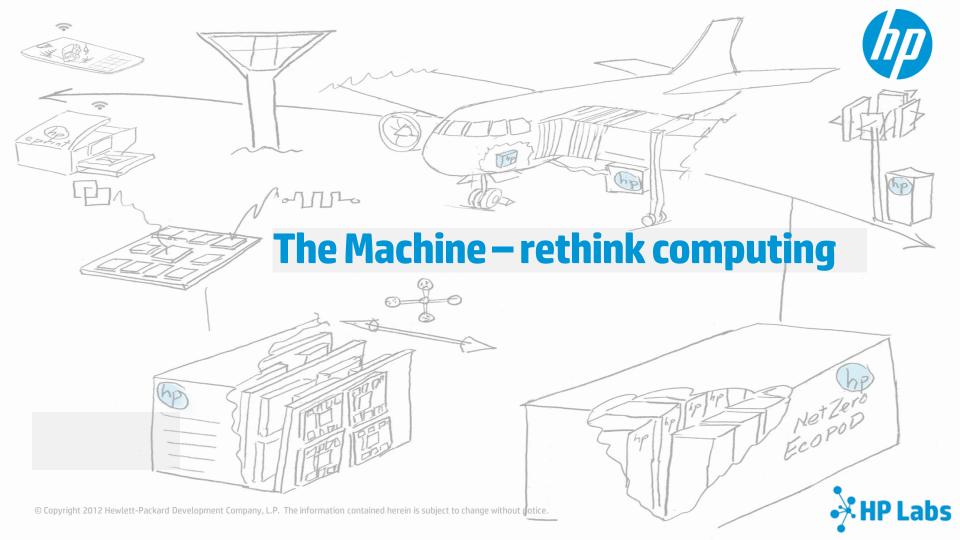


## 6 words to summarize the vision

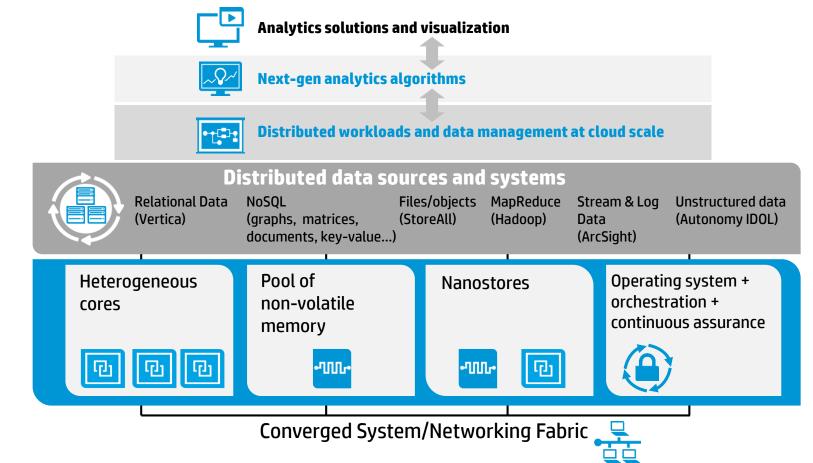


## Not substitutional technologies Holistic re-architecting to get all benefits



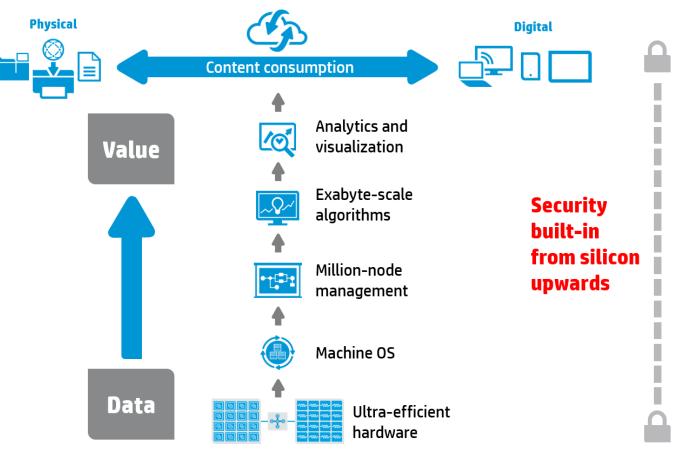


## New architecture enables fundamental changes



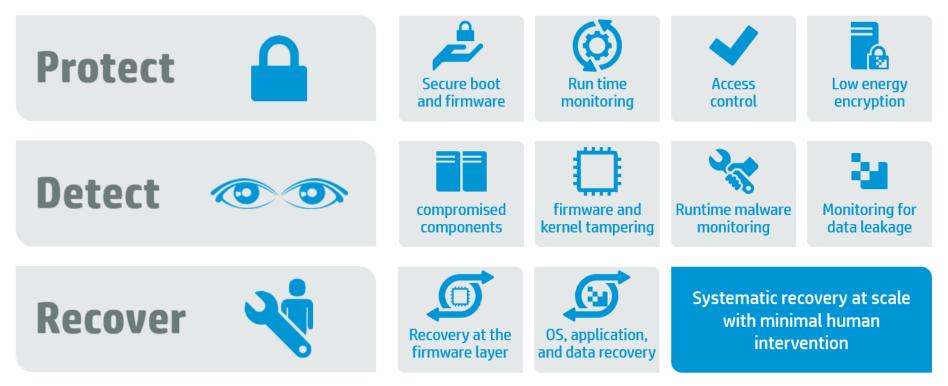


## The Machine: towards a new computing paradigm



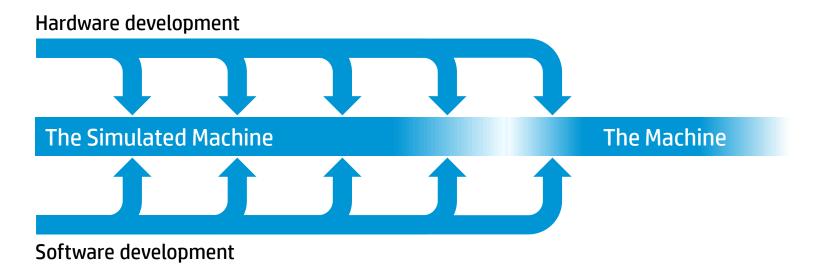


# Security framework





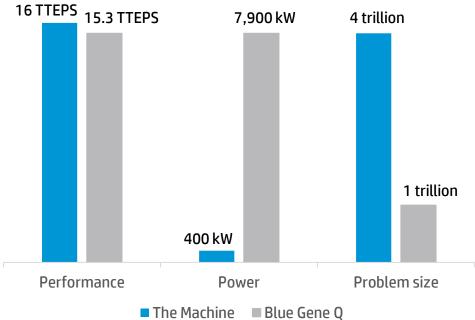
# Hardware/software co-development





# Performance estimates – graph traversal

What could you do if you could traverse 16 trillion graph edges per second?



#### Graph 500-like workload

#### Sequoia, Blue Gene Q at Livermore

64,000 nodes, > 1M cores total

#### HP – The Machine

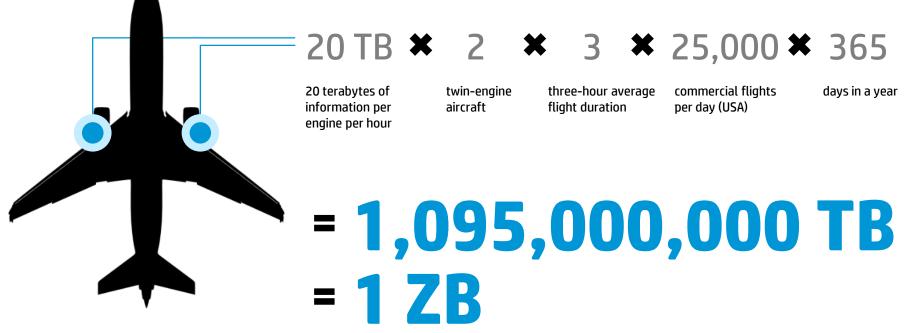
20 racks, 256 SoCs / rack, 122k cores total

256 GB NVM per SoC, 1.3 PB total 256 NICs per rack, 2\*100 Gbps links / NIC Utilization < 70%



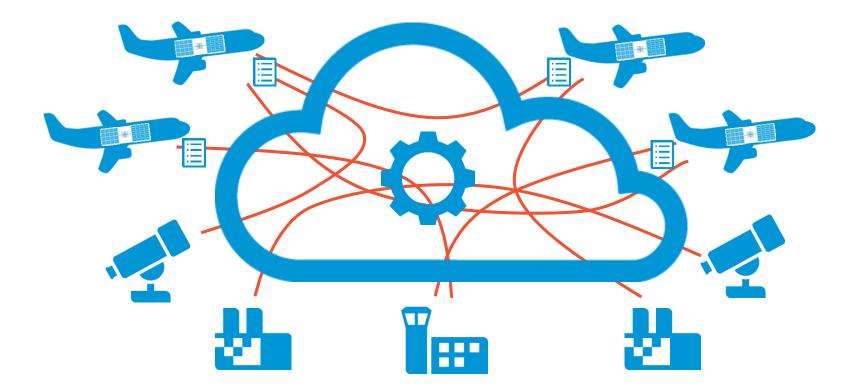
## Use case: aircraft sensors

Internet-of-Things big data affects all industries





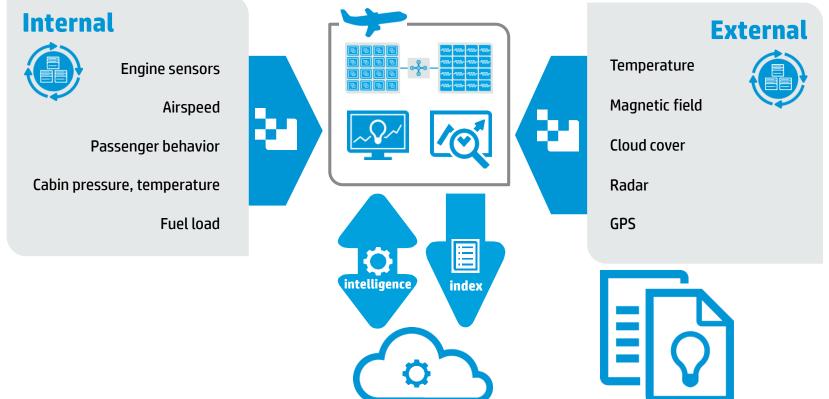
## Use case: a mesh of connected aircrafts ...





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# Use case: the analytical aircraft





# Aspirational History

	<ul> <li>SoC Partners co-developn</li> <li>Machine OS begins</li> </ul>	<ul> <li>Memristors</li> <li>Physical infr prototypes</li> <li>Open Source emulators r</li> </ul>	e Machine OS SE	ore )K and	-	eleased • Core de • Machin product as a bus	
<b>***</b> **	2014	2015	2016	2017	2018	2019	2020
•MU- •MU-			<ul> <li>Memristor launched</li> <li>Integrated</li> </ul>				Distributed mesh compute goes mainstream
-MUMUMU-			technolog	ies			
$\begin{array}{c} -\mathbf{U}\mathbf{U}\mathbf{v} & -\mathbf{U}\mathbf{U}\mathbf{v} & -\mathbf{U}\mathbf{U}\mathbf{v} \\ -\mathbf{U}\mathbf{U}\mathbf{v} & -\mathbf{U}\mathbf{U}\mathbf{v} & -\mathbf{U}\mathbf{U}\mathbf{v} \end{array}$					es begin sampling enters public beta		

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# The MACHINE .....



The Machine Webpage

The Machine 3 min video

Memristor Lab Tour

**Photonics Lab Tour** 

**HP Analytics Lab** 

**HP Security and Cloud Lab** 



